Amendments to the Claims

This listing of claims replaces all prior versions and listings of claims in the application.

Listing of Claims

1. (Currently Amended) A semiconductor device comprising:

a semiconductor having at least channel, source and drain regions;

an insulating film formed on said semiconductor;

a gate electrode over the insulating film;

a first interlayer insulating film over said insulating film and the gate electrode;

a second interlayer insulating film on said first interlayer insulating film, said second interlayer insulating film comprising a different material from said insulating film;

a first opening in said insulating film for exposing a portion of said semiconductor;

a second opening in said first interlayer insulating film for exposing said portion of said semiconductor layer and a portion of said insulating film **[[where]]** that surrounds said first opening; and

a third opening in said second interlayer insulating film for exposing said portion of said semiconductor, said portion of said insulating film and a portion of said first interlayer insulating film **[[where]]** that surrounds said second opening,

wherein edges of at least said third opening are rounded off, and

wherein a thickness of the first interlayer insulating film is less than one third of a total thickness of the first and second interlayer insulating films.

2. (Previously Presented) A device according to claim 1 wherein a taper angle β of the second interlayer insulating film with respect to a major surface of said semiconductor in the third opening is larger than a taper angle α of the first interlayer insulating film with respect to the major surface of said semiconductor in the second opening.

3. (Previously Presented) A device according to claim 1, wherein said insulating film comprises silicon oxide.

4. (Previously Presented) A device according to claim 1, wherein said first and second interlayer insulating films comprise a material selected from the group consisting of silicon nitride and organic resin.

5. (Previously Presented) A device according to claim 1, wherein said second interlayer insulating film has a dry etching rate higher than said first interlayer insulating film.

6. (Currently Amended) A semiconductor device comprising:

a semiconductor layer formed over a substrate having an insulating surface, said semiconductor layer having at least channel, source and drain regions;

a gate insulating film over said semiconductor layer;

a gate electrode over the gate insulating film;

a first interlayer insulating film over said gate insulating layer and the gate electrode

a second interlayer insulating film on said first interlayer insulating film, said second interlayer insulating film comprising a different material from said gate insulating film;

a first opening in said gate insulating film for exposing a portion of said semiconductor layer;

a second opening in said first interlayer insulating film for exposing said portion of said semiconductor layer and a portion of said gate insulating film **[[where]]** <u>that</u> surrounds said first opening; and

a third opening in said second interlayer insulating film for exposing said portion of said semiconductor layer, said portion of said gate insulating film and a portion of said first interlayer insulating film **[[where]]** <u>that</u> surrounds said second opening,

wherein edges of at least said third opening are rounded off, and

wherein a taper angle β of the second interlayer insulating film with respect to a major surface of said semiconductor layer in the third opening is larger than a taper angle α of the first interlayer insulating film with respect to the major surface of said semiconductor layer in the second opening.

7. (Previously Presented) A device according to claim 6, wherein said gate insulating film comprises silicon oxide.

8. (Previously Presented) A device according to claim 6, wherein said first and second interlayer insulating film comprise a material selected from the group consisting of silicon nitride and organic resin.

9. (Previously Presented) A device according to claim 6, wherein said second interlayer insulating film has a dry etching rate higher than said first interlayer insulating film.

10. (Currently Amended) A semiconductor device comprising:

a semiconductor having at least channel, source and drain regions;

an insulating film on said semiconductor;

a gate electrode over the insulating film;

a first interlayer insulating film over said insulating film and the gate electrode;

a second interlayer insulating film on said first interlayer insulating film;

a first opening in said insulating film for exposing a portion of said semiconductor;

a second opening in said first interlayer insulating film for exposing said portion of said semiconductor and a portion of said insulating film **[[where]]** that surrounds said first opening;

a third opening in said second interlayer insulating film for exposing said portion of said semiconductor, said portion of said insulating film and a portion of said first interlayer insulating film **[[where]]** that surrounds said second opening; and

an electrode formed on said first, second, and third openings and connected with one of said source and drain regions through said first, second, and third openings,

wherein a taper angle β of the second interlayer insulating film with respect to a major surface of said semiconductor in the third opening is larger than a taper angle α of the first interlayer insulating film with respect to a major surface of said semiconductor in the second opening, and

wherein a thickness of the first interlayer insulating film is less than one third of a total thickness of the first and second interlayer insulating films.

11. (Previously Presented) A device according to claim 10, wherein said insulating film comprises silicon oxide.

12. (Previously Presented) A device according to claim 10, wherein said first and second interlayer insulating film comprise a material selected from the group consisting of silicon nitride and organic resin.

13. (Previously Presented) A device according to claim 10, wherein said second interlayer insulating film has a dry etching rate higher than said first interlayer insulating film.

14. (Currently Amended) A semiconductor device comprising:

a semiconductor layer formed over a substrate having an insulating surface and including at least channel, source and drain regions;

an insulating film on said semiconductor layer;

a gate electrode over the insulating film;

at least a first interlayer insulating film over the insulating film and over the gate electrode, and a second interlayer insulating film over ~~said insulating film and the gate electrode~~ the first interlayer insulating film;

at least one contact hole in said first and second interlayer insulating films and said insulating film, said contact hole having a tapered section; and

an electrode formed on said contact hole and connected with one of said source and drain regions through said contact hole,

wherein a taper angle β of an inner surface of the second interlayer insulating film in the contact hole with respect to a major surface of said semiconductor layer is larger than a taper angle α of an inner surface of the first interlayer insulating film in the contact hole with respect to said major surface of said semiconductor layer.

15. (Previously Presented) A device according to claim 14, wherein said insulating film comprises silicon oxide.

16. (Previously Presented) A device according to claim 14, wherein said first and second interlayer insulating film comprise a material selected from the group consisting of silicon nitride and organic resin.

17. (Previously Presented) A device according to claim 14, wherein said second interlayer insulating films has a dry etching rate higher than said first interlayer insulating layer.

18. (Previously Presented) A device according to claim 14, wherein angles of the tapered section of the contact hole decrease successively from the second interlayer insulating layer toward a first interlayer insulating layer.

19. (Currently Amended) A semiconductor device comprising:

a semiconductor having a channel region, at least one low doped impurity region, and at least one high doped impurity region said high doped impurity region being adjacent to said channel region with said low doped impurity region interposed therebetween;

an insulating film on said semiconductor;

a gate electrode over the insulating film;

at least a first interlayer insulating film over the insulating film and over the gate electrode, and a second interlayer insulating **[[films]]** film over ~~said insulating film and the gate electrode~~ the first interlayer insulating film; and

a contact hole in said first and second interlayer insulating films and said insulating film for exposing a portion of said high doped impurity region, said contact hole including a first hole in the second interlayer insulating film, a second hole in the first interlayer insulating film, and a third hole in the insulating film, the contact hole having **[[has]]** a tapered section such that the first hole has a larger cross section than the second hole, and the second hole has a larger cross section than the third hole,

wherein edges of said second interlayer insulating film in said contact hole are rounded off,

wherein angles of the tapered section of the contact hole decrease successively from the second interlayer insulating film toward the first interlayer insulating film, and

wherein a thickness of the first interlayer insulating film is less than one third of a total thickness of the first and second interlayer insulating films.

20. (Previously Presented) A device according to claim 19 wherein said insulating film comprises silicon oxide.

21. (Currently Amended) A device according to claim 19 wherein at least one of said first and second interlayer insulating films comprises a material selected from the group consisting of silicon nitride and organic resin.

22. (Previously Presented) A device according to claim 19 wherein said low doped impurity region includes phosphorus at a dose of 0.1 to 5 x 10^{14} atoms/cm^2.

23. (Previously Presented) A device according to claim 19 wherein said high doped impurity region includes phosphorus at a dose of 0.2 to 5 x 10^{15} atoms/cm^2.

24. (Currently Amended) A semiconductor device comprising:

a semiconductor layer formed over a substrate having an insulating surface and having a channel region, at least one low doped impurity region, and at least one high doped impurity region said high doped impurity region being adjacent to said channel region with said low doped impurity region interposed therebetween;

an insulating film on said semiconductor layer;

a gate electrode over the insulating film;

at least a first interlayer insulating film over the insulating film and over the gate electrode, and a second interlayer insulating **[[films]]** film over ~~said insulating film and the gate electrode~~ the first interlayer insulating film; **[[and]]**

a contact hole in said interlayer insulating films and said insulating film for exposing a portion of said high doped impurity region, said contact hole has a tapered section; and

an electrode formed on said contact hole and connected with one of said source and drain regions through said contact hole,

wherein edges of said interlayer insulating film in said contact hole are rounded off.

25. (Previously Presented) A device according to claim 24, wherein a taper angle β of an inner surface of the second interlayer insulating film in the contact hole with respect to a major surface of said semiconductor layer is larger than a taper angle α of an inner surface of first interlayer insulating film in the contact hole with respect to said major surface of said semiconductor layer.

26. (Previously Presented) A device according to claim 24, wherein angles of the taper shape of the contact hole decrease successively from the second interlayer insulating film toward the first interlayer insulating film.

27. (Previously Presented) A device according to claim 24 wherein said insulating film comprises silicon oxide.

28. (Currently Amended) A device according to claim 19 wherein at least one of said first and second interlayer insulating films comprises a material selected from the group consisting of silicon nitride and organic resin.

29. (Previously Presented) A device according to claim 24 wherein said low doped impurity region includes phosphorus at a dose of 0.1 to 5 x 10^{14} atoms/cm^2.

30. (Previously Presented) A device according to claim 24 wherein said high doped impurity region includes phosphorus at a dose of 0.2 to 5 x 10^{15} atoms/cm^2.

31. (Previously Presented) A device according to claim 1, wherein edges of said first opening are rounded off.

32. (Previously Presented) A device according to claim 1, further comprising an electrode connected with one of said source and drain regions through said first, second, and third openings.

33. (Previously Presented) A device according to claim 6, wherein edges of said first opening are rounded off.

34. (Previously Presented) A device according to claim 6, further comprising an electrode connected with one of said source and drain regions through said first, second, and third openings.

35. (Previously Presented) A device according to claim 19, wherein edges of said insulating film in said contact hole are rounded off.

36. (Previously Presented) A device according to claim 19, further comprising an electrode connected with one of said source and drain regions through said contact hole.

37. (Previously Presented) A device according to claim 24, wherein edges of said insulating film in said contact hole are rounded off.

38. (Currently Amended) A device according to claim 6, wherein a thickness of the first interlayer insulating film is less than one third of a total thickness of the first and second interlayer insulating films.

39. (Currently Amended) A device according to claim 14, wherein a thickness of the first interlayer insulating film is less than one third of a total thickness of the first and second interlayer insulating films.

40. (Currently Amended) A device according to claim 24, wherein a thickness of the first interlayer insulating film is less than one third of a total thickness of the first and second interlayer insulating films.

41. (New) A device according to claim 14, wherein said first interlayer insulating film is formed on and in contact with the insulating film, and over the gate electrode, and said second interlayer insulating film is formed on and in contact with said first interlayer insulating film.

42 (New) A device according to claim 19, wherein said first interlayer insulating film is formed on and in contact with the insulating film, and over the gate electrode, and said second interlayer insulating film is formed on and in contact with said first interlayer insulating film.

43. (New) A device according to claim 24, wherein said first interlayer insulating film is formed on and in contact with the insulating film, and over the gate electrode, and said second interlayer insulating film is formed on and in contact with said first interlayer insulating film.